17/12 GHz COMMUNICATION RECEIVER FOR DIRECT BROADCAST SATELLITES

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Abstract

This paper describes the design and performance of a 17/12 GHz Communication Receiver for the first US Direct Broadcast Satellite (DBS) to be launched in 1986. The receiver has an operating bandwidth of 500 MHz, a maximum noise figure of 6.0 dB (at 60°C), small-signal gain of 35 dB (nominal), gain stability of 0.5 dB peak-to-peak and a third-order intercept point of 26 dBm (minimum) when operated over -10°C to 60°C temperature range. Measured data on a development model receiver are presented.

Introduction

The 17/12 GHz Communication Receiver down-converts the Direct Broadcast Satellite's (DBS) uplink frequency band (17.3-17.8 GHz) to the downlink frequency band (12.2-12.7 GHz) with high frequency stability. It also provides low noise performance, high linearity and distortionless transmission characteristics such as low crosstalk, low-level spurii, small group delay variation and negligible AM/PM conversion.

Receiver Description

The receiver is an all solid-state and compact MIC design using space-qualified parts and fabrication techniques. A block diagram of the receiver is shown in Figure 1.

The design of the receiver consists of the following three subassemblies:

- RF (or Microwave) Unit
- Local Oscillator Unit
- DC/DC Converter Unit

The three units are bolted together to form the receiver 'box' as shown in Figure 2. The other key design features of the receiver are:

- Computer-Aided Design of all the microwave and RF circuits.
- Drop-in module concept for maximum flexibility in production and testing.
- Compartmented gold-plated magnesium housings for minimum volume and weight.
- Easy access to the RF and LO circuits for final alignment.
- Temperature compensation for gain stability using simple thermistor networks.
- Test ports for alignment and trouble-shooting.

RF Unit Design and Description

A detailed block and level diagram of the RF unit is shown in Figure 1. The unit essentially consists of the following microwave modules:

- A well-matched (VSWR $\leq$ 1.15:1) 17 GHz input isoadaptor which provides a low loss ($\leq$ 0.3 dB) WR62-to-SMA transition.
- Two dual-stage low noise amplifiers (LNAs) using NE67383 GaAs FET devices. The dual stage amplifier is designed and optimized using 'SUPERCOMPACT' for low noise and high gain performance. In addition, the DC decoupling networks of the gate and drain bias ports are designed and optimized to provide > 25 dB bandstop rejection of the image frequency band (7.1 to 7.6 GHz). Figure 3 shows the measured inband gain and noise figure response of the dual-stage amplifier. Figure 4 shows the measured and computed wideband response of the amplifier, including the image rejection response. The dual stage amplifier has a maximum noise figure of 3.8 dB, a nominal gain of 12.0 dB over 17 to 18 GHz band and an image rejection of > 28 dB.
- A 17 GHz 14 dB coupler follows the low noise amplifiers and provides a test port for the alignment of the amplifiers.
- A 17/12 GHz hermetically sealed 'drop-in' double-balanced mixer provides the downconversion. The mixer has a conversion loss of 7.0 dB and a noise figure of 7.5 dB.
- A 12 GHz coupled-line MIC bandpass filter follows the mixer. The filter is a seven section 0.01 dB Chebyschev design and provides attenuation of the local oscillator harmonics and out-of-band mixing products. A 12 GHz 14 dB coupler follows the filter and is located on the same substrate. The filter/coupler combination has an insertion loss of 3.0 dB with 0.25 dB peak-to-peak flatness over 12.2 to 12.7 GHz band.
- A dual-stage 12 GHz HFET-2201 GaAs FET amplifier with a noise figure of 4.0 dB, nominal

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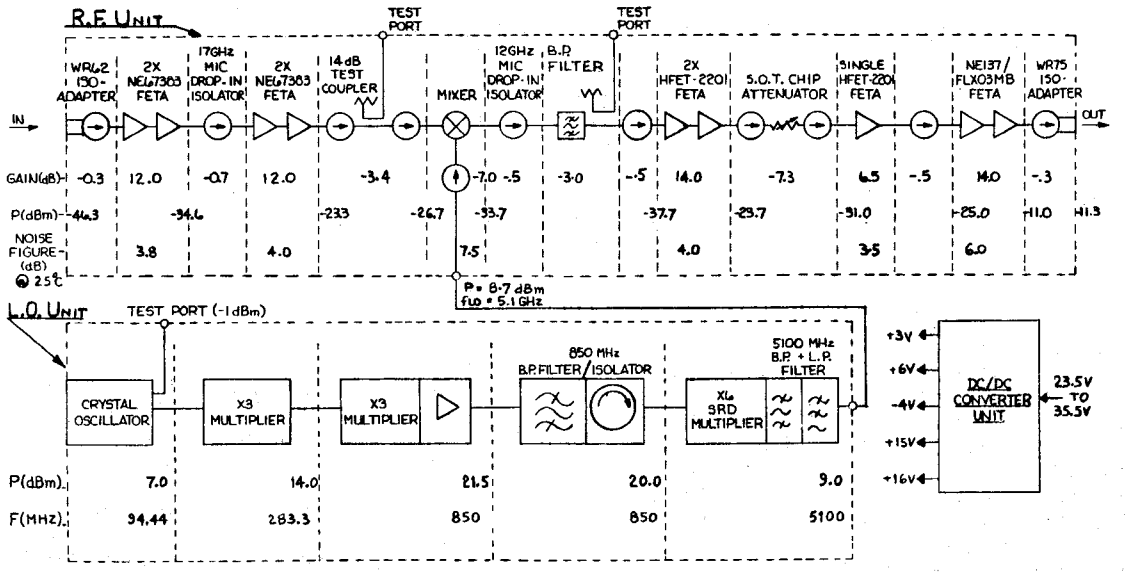

Figure 1. Block Diagram of the Receiver

gain of 14.0 dB and gain flatness of 0.25 dB p-p over 12.2 to 12.7 GHz band.

- A level set chip attenuator which is used to set the receiver gain to 35 dB nominal.
- A single-stage HFET-2201 amplifier with a noise figure of 3.5 dB, a gain flatness of 0.25 dB p-p over 12.2 to 12.7 GHz band.
- A dual stage output amplifier which uses a NE13783 GaAs FET driving a FLX03MB GaAs FET. The amplifier has a gain of 14 dB, gain flatness of 0.25 dB p-p and a third-order intercept point of 30 dBm (minimum) over 12.2 to 12.7 GHz band. The output stage provides a minimum third-order intercept point of 26 dBm for the overall receiver.
- A well-matched (VSWR $\leq$ 1.15:1) 12 GHz output isoadaptor provides a low loss ($\leq$ 0.3 dB) transition from SMA to WR75 waveguide.

'Drop-in' ferrite isolators are used between various microwave modules to achieve good match and high isolation which results in ripple-free gain response.

The modules are fabricated using alumina substrates soldered to gold-plated Kovar carriers. The modules are mounted inside a gold-plated compartmented RF housing and interconnected with gold ribbon bonds. The housing has an H-frame cross-section. The backside of the housing is used for the DC bias circuits. Gasketed gold-plated covers are placed on both sides of the housing to achieve good EMI performance.

Local Oscillator Design and Description

A block diagram of the local oscillator unit is shown in Figure 1. The unit consists of the following circuit modules:

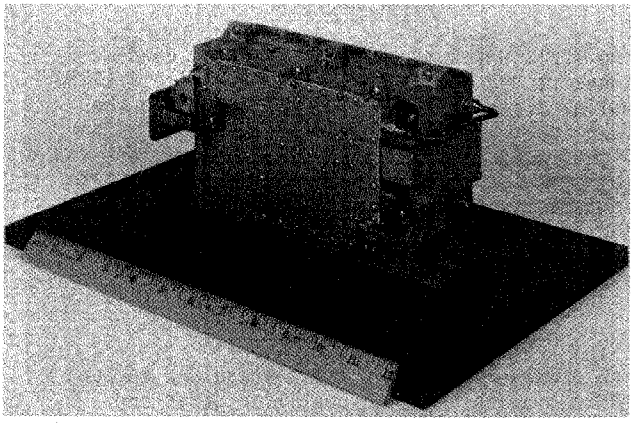

Figure 2. Photograph of the Receiver

- A 94.4 MHz crystal oscillator with an oven-stabilized crystal to achieve high frequency stability over life and temperature.
- An X3 transistor multiplier with saturated output of 14 dBm to drive the second X3 multiplier.
- An X3 multiplier and amplifier circuit with a saturated output power of 21 dBm to drive the X6 Step Recovery Diode (SRD) output multiplier.
- A low loss (1.2 dB) 850 MHz four section combline filter with a 3 dB bandwidth of 70 MHz to provide adequate suppression (-80 dBc) of unwanted harmonics of 850 MHz.
- An isolator-coupled X6 SRD multiplier with an output power of 11 dBm at 5.1 GHz.
- A MIC bandpass/low-pass filter combination, with an insertion loss of 2.5 dB, to filter the unwanted harmonics of 5.1 GHz at the local oscillator output.

All the local oscillator circuits are housed inside a compact compartmented gold-plated housing. A gasketed gold-plated cover provides the required EMI shielding.

DC/DC Converter Design

The unregulated 36V spacecraft bus voltage is converted to the required voltages (see Figure 1) by a transformer-coupled DC-to-DC converter operating as a pulse-width modulated switching regulator. The primary winding of the transformer is driven by a pulse width modulator running at 50 KHz. The secondary windings are designed to provide optimum half-wave rectification, series regulation and low-pass filtering to recover the DC voltages. The converter circuit board is housed inside of a separate gold-plated housing. DC interconnections to the RF and LO units are provided via filtercons.

Measured Performance

A development model receiver was integrated, aligned and tested at ambient temperature and in thermal-vacuum over the qualification temperature range of -10°C to 60°C. Table 1 summarizes the worst-case measured performance. Figure 5 shows the measured gain and noise figure data at -10°C, 25°C and 60°C in thermal vacuum. The unit was vibrated in all three axes (sine and random) up to 20 G's. Post-vibration and pre-vibration measurements of gain and noise figure response were in agreement. The results indicate that receiver offers excellent transmission characteristics and stable performance in its operating environment.

Table 1

Performance Summary of the Development Model 17/12 GHz Communication Receiver

Parameter	Measured Value
Input/Output Frequency Bands	17.3-17.8/12.2-12.7
Max. Noise Figure	6.0
Nominal Gain, dB	35
Gain Flatness, dB p-p	0.5
Gain Slope, dB/MHz	0.005
Gain Stability, dB p-p	0.5
Frequency Stability, ppm	± 0.9
Group Delay, ns/28 MHz	.38
AM/PM Conversion deg/dB	0.05
Phase Shift, Degrees	0.3
Third Order Intercept Point, dBm	26
DC Power Consumption (in vacuum), watts	5.7 (at V_{bus} = 35.5V)
Input/Output VSWR	1.06:1/1.15:1
Size, inches	9.27 x 3.75 x 4.9
Weight, lbs.	3.3
Temperature, °C	-10 to 60

Acknowledgements

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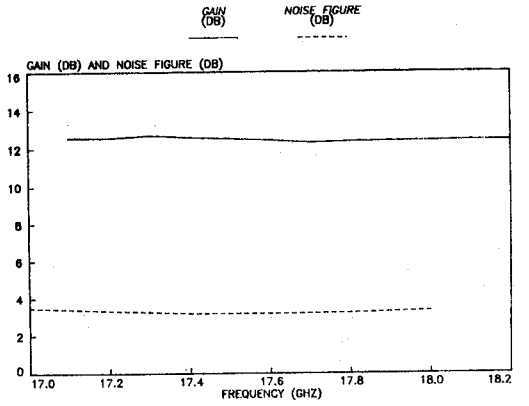

Figure 3. Typical Inband Response of 17 GHz Dual-Stage LNA

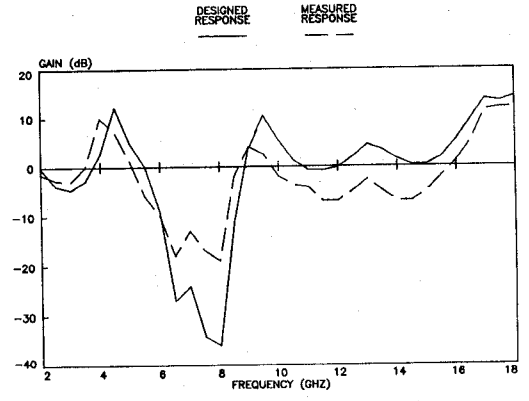

Figure 4. Typical Wideband Response of 17 GHz Dual-Stage LNA

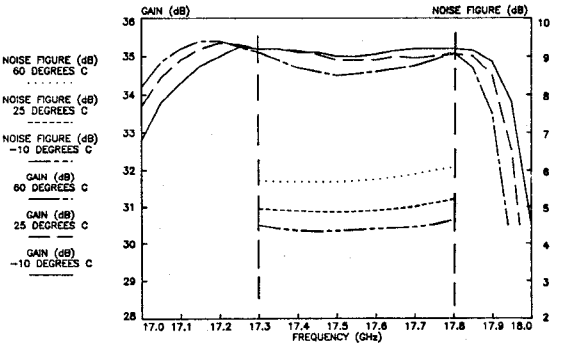

Figure 5. Noise Figure/Gain Response of the Development Model Receiver in Vacuum